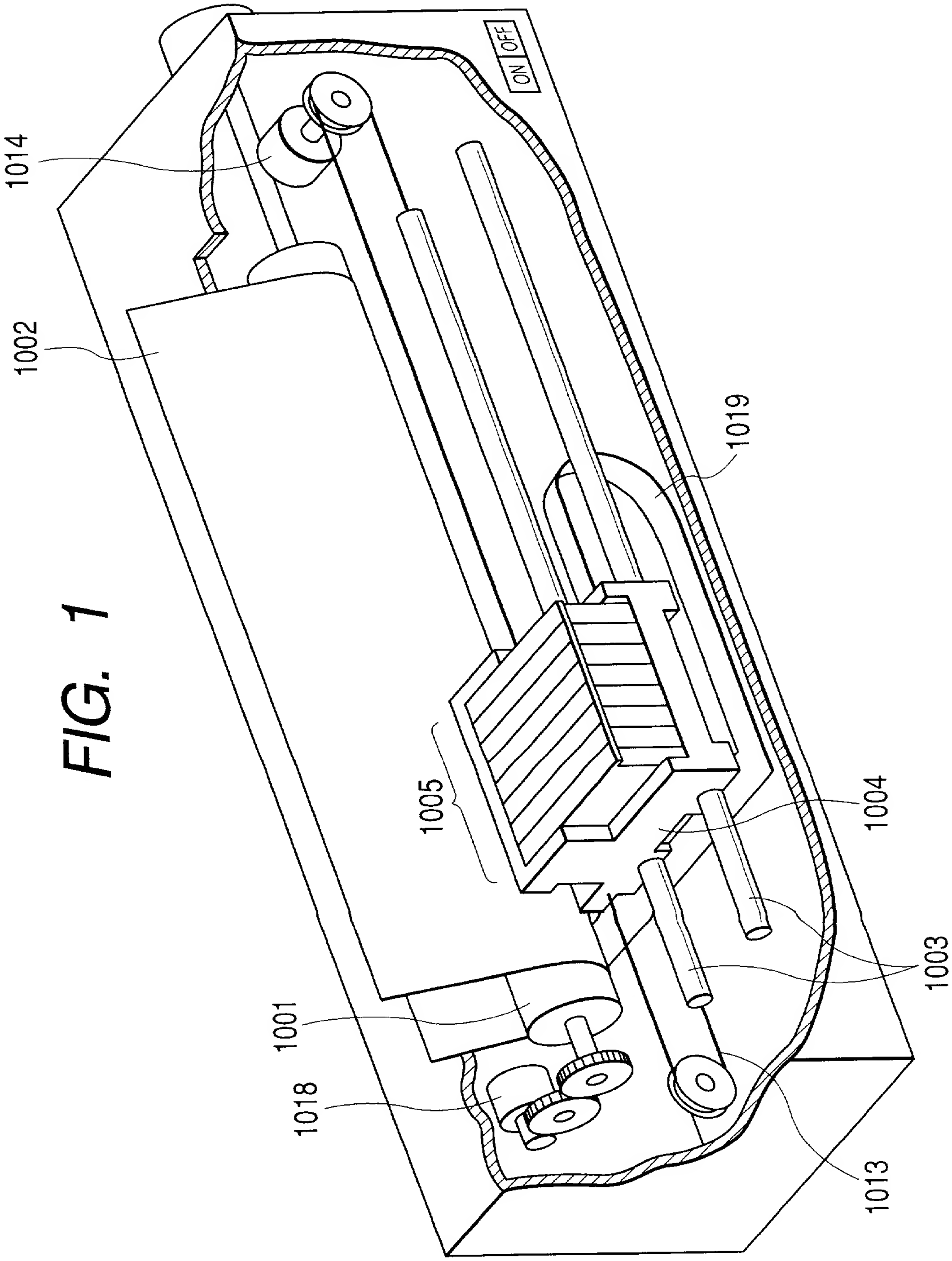


FIG. 1

FIG. 2

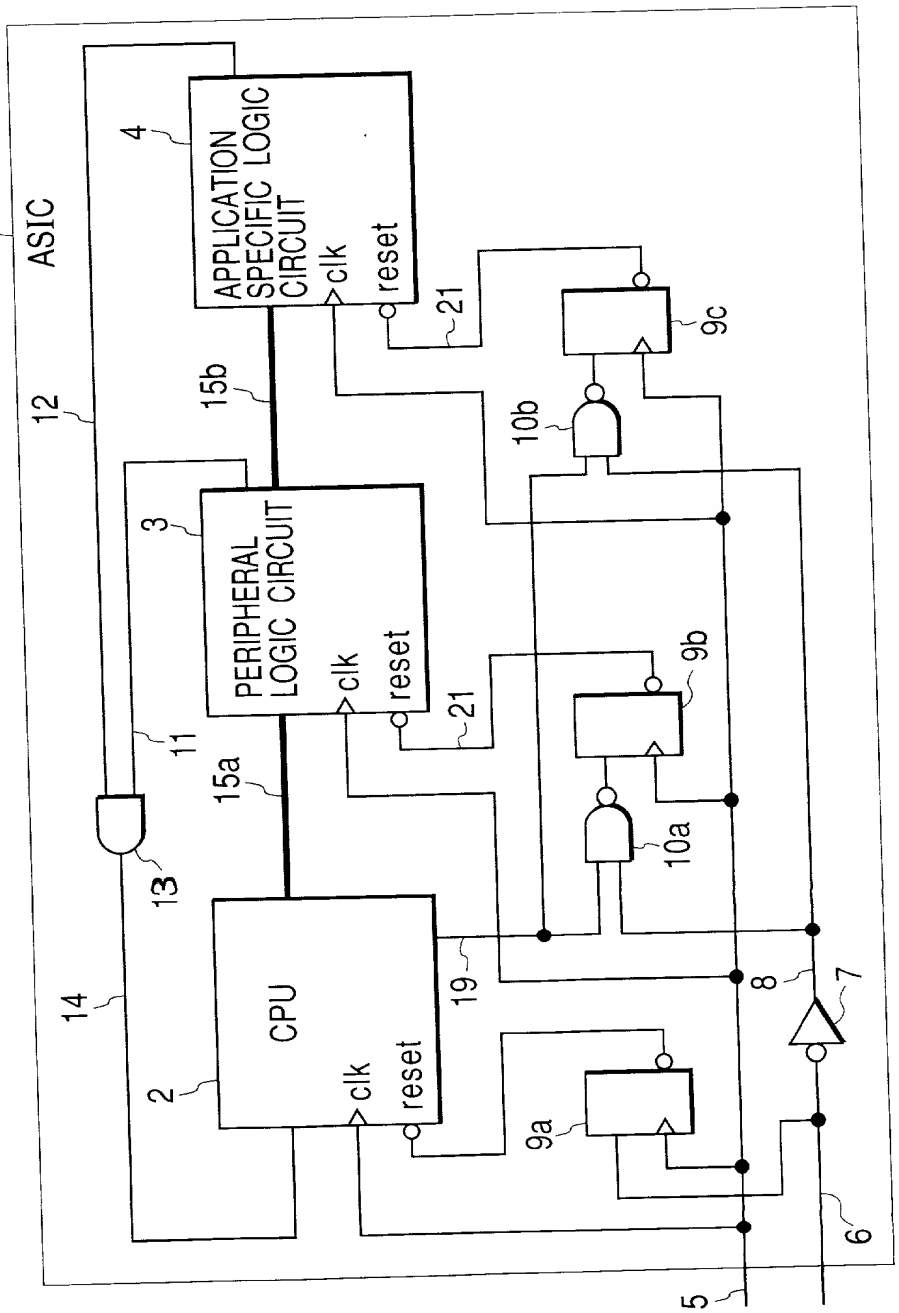

1
ASIC
4
APPLICATION SPECIFIC LOGIC CIRCUIT
clk
reset
21
9c
15b
12
10b
3
PERIPHERAL LOGIC CIRCUIT
clk
reset
21
9b
11
15a
10a
13
14
2
CPU
clk
reset
19
8
7
9a
6
5

FIG. 3

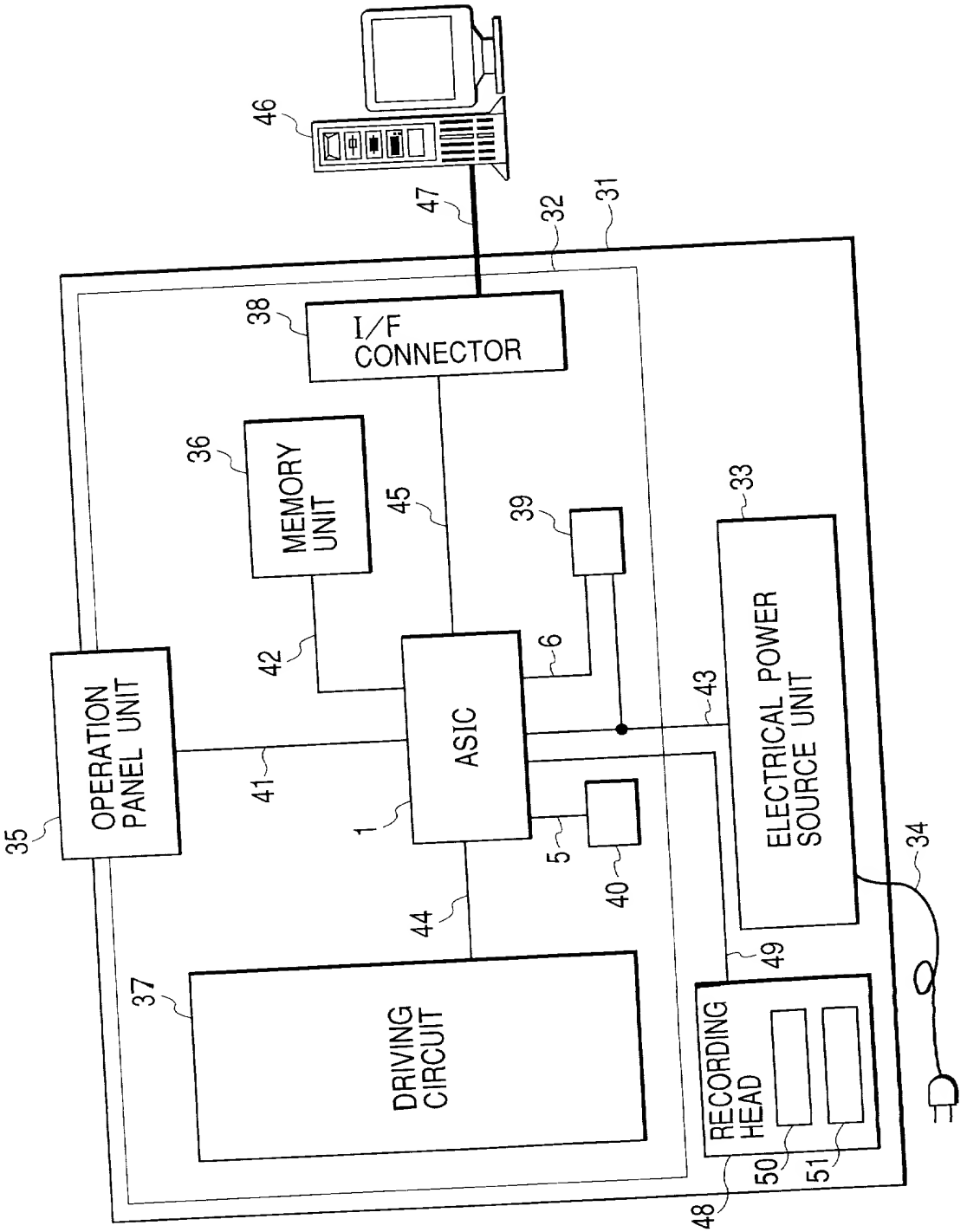

46
47
32
31
38
I/F CONNECTOR
36
MEMORY UNIT
45
39
33
42
6
43
ELECTRICAL POWER SOURCE UNIT
OPERATION PANEL UNIT
41
ASIC
35
1
5
40
34
44
49
37
DRIVING CIRCUIT
RECORDING HEAD
48
50
51

FIG. 4

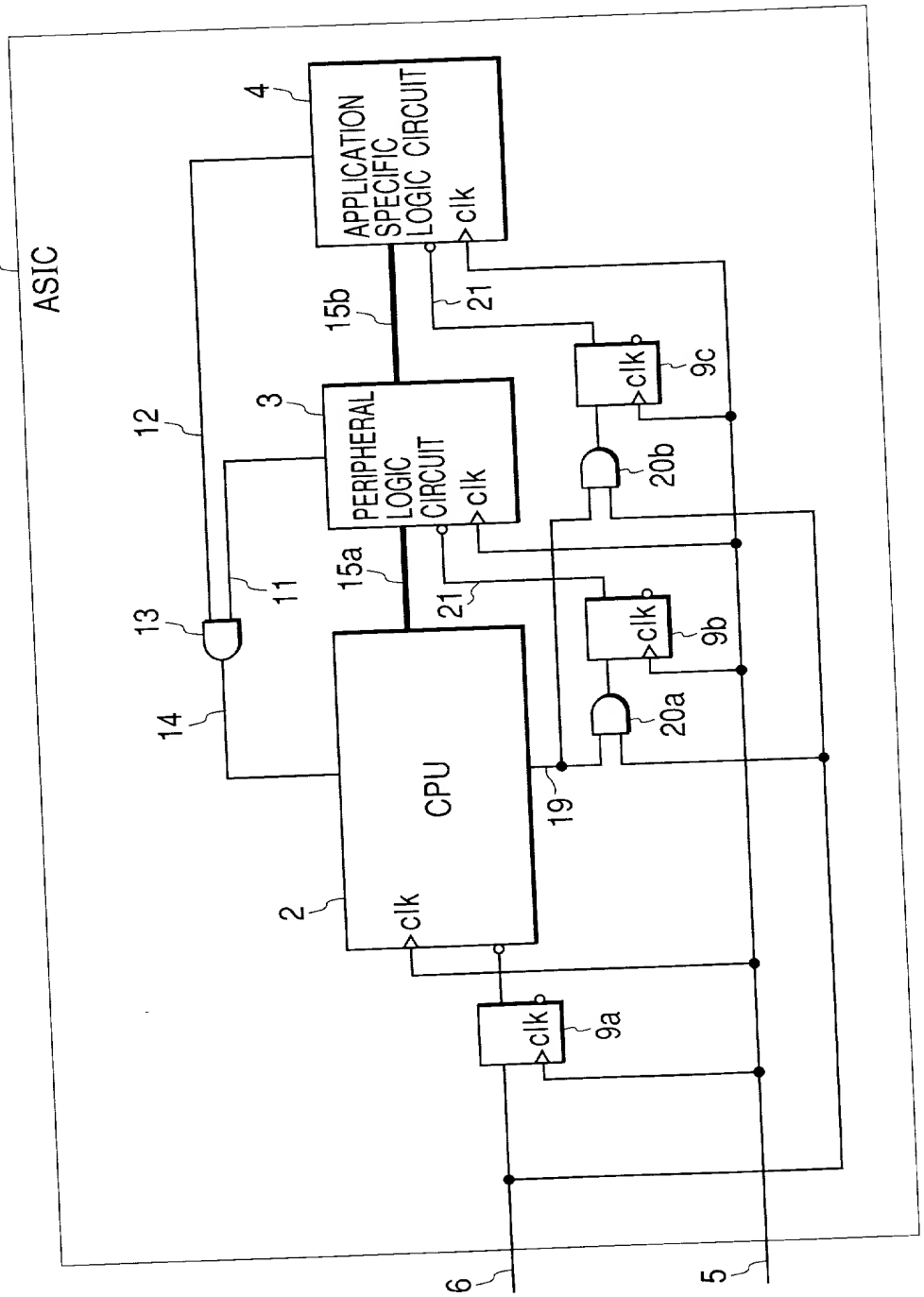

1
ASIC
4
APPLICATION SPECIFIC LOGIC CIRCUIT
clk
15b
21
3
PERIPHERAL LOGIC CIRCUIT
clk
12
15a
21
11
13
14
2
CPU
clk
19
clk
9a
clk
9b
clk
9c
20a
20b
6
5

FIG. 5

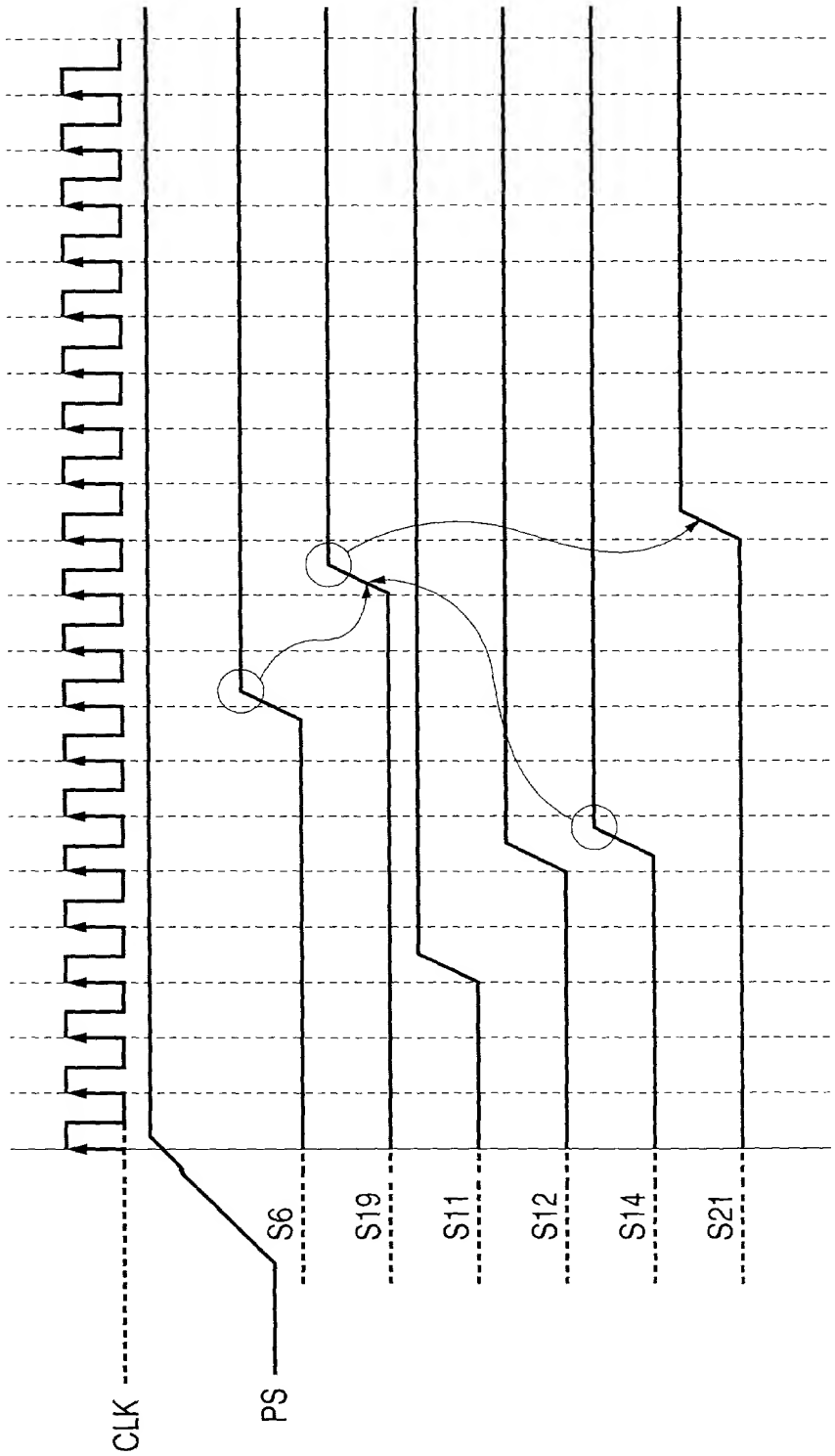


FIG. 6

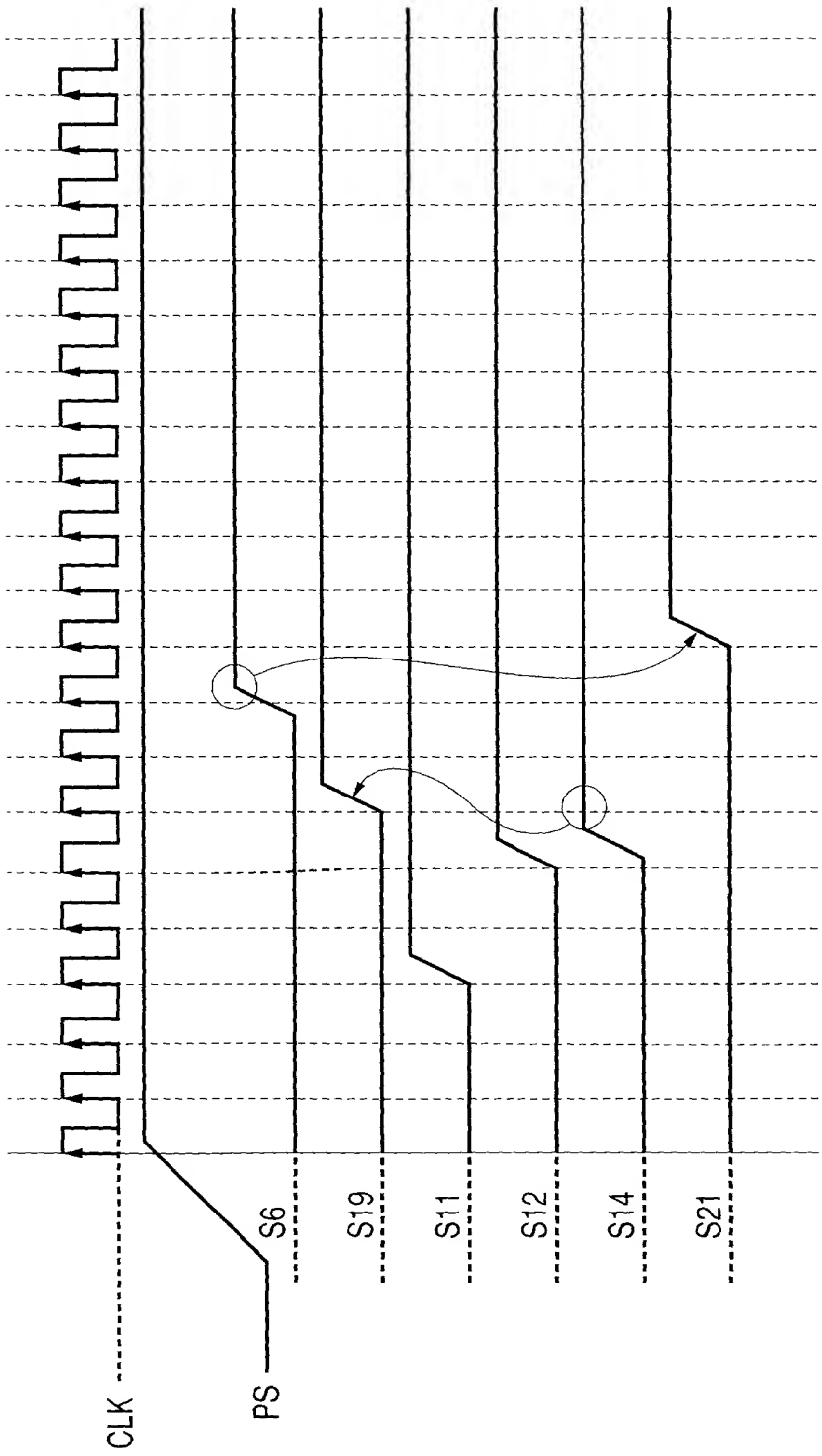


FIG. 7

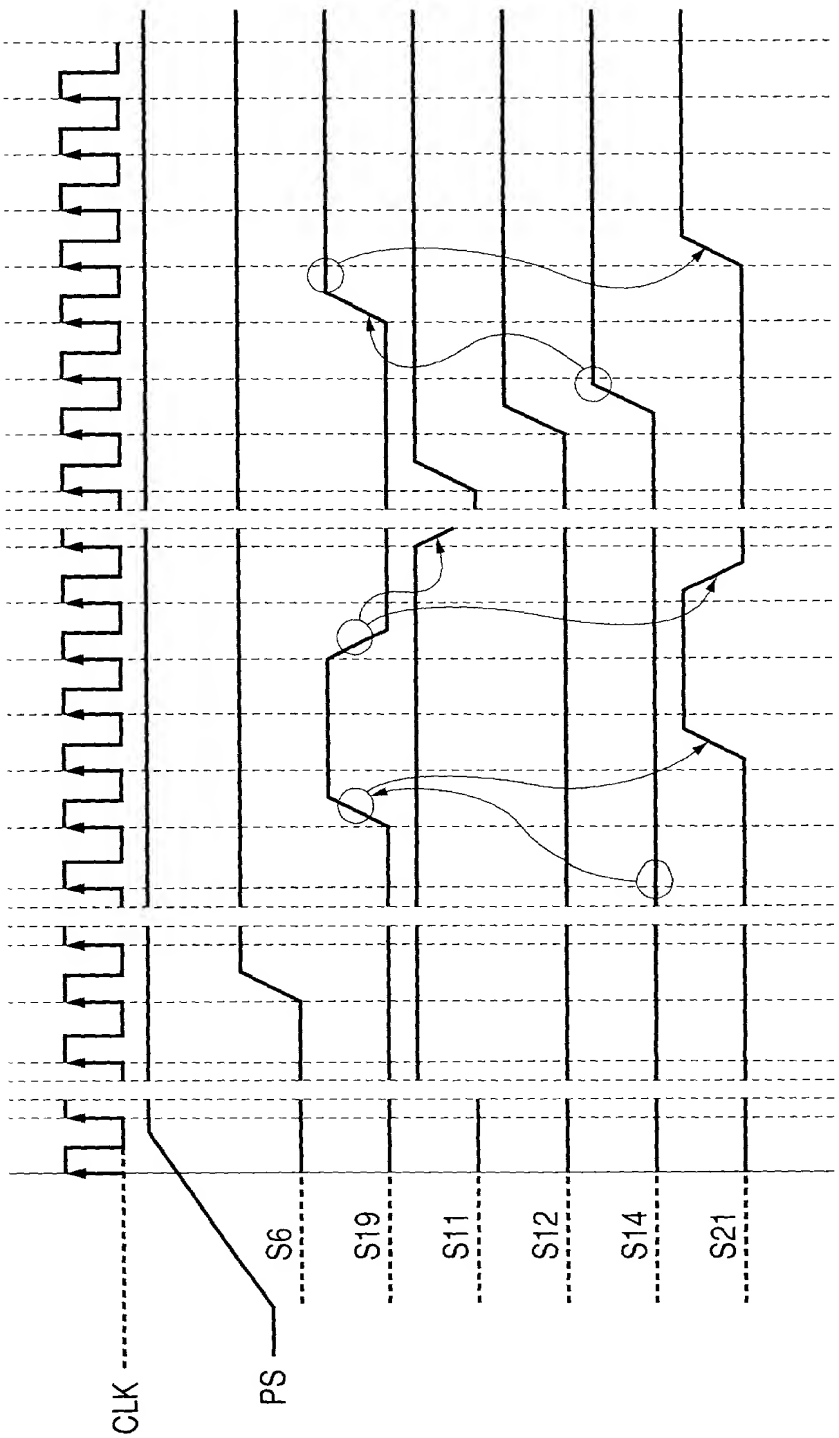


FIG. 8

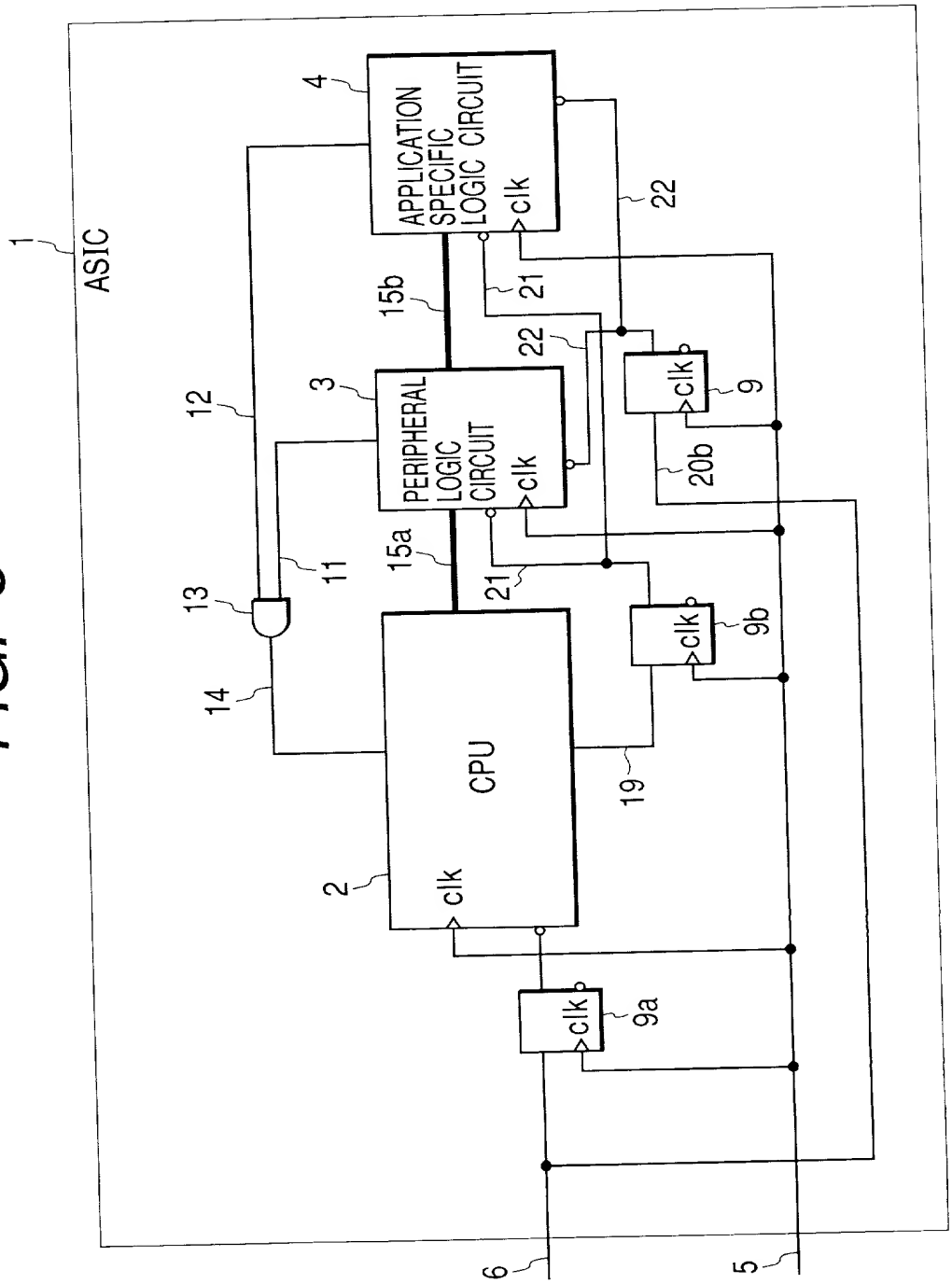

1
ASIC
4
APPLICATION SPECIFIC LOGIC CIRCUIT
clk
22
21
15b
3
PERIPHERAL LOGIC CIRCUIT
clk
12
22
clk
9
20b
13
11
15a
21
clk
9b
14
CPU
19
2
clk
clk
9a
6
5

FIG. 9

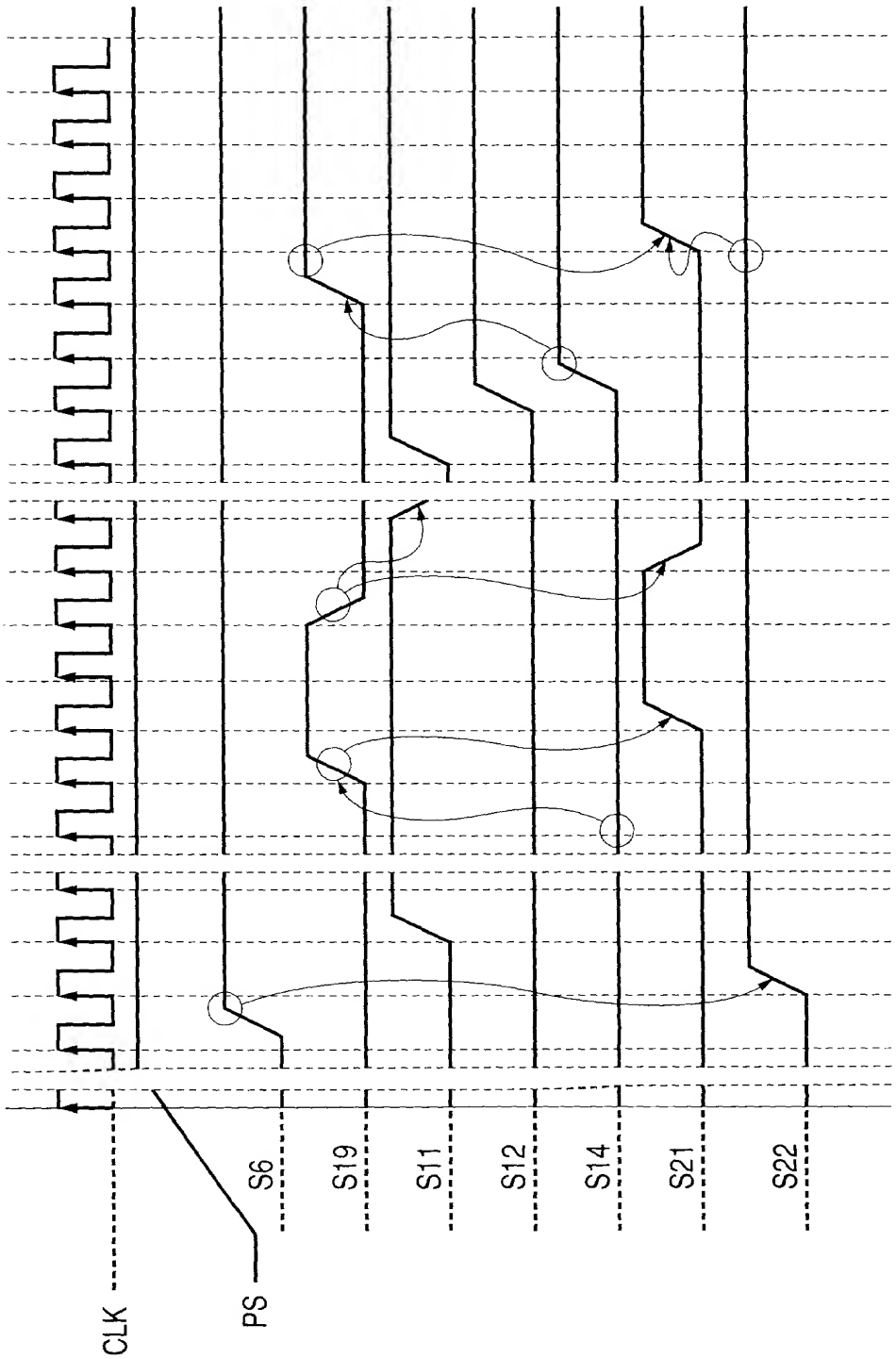


FIG. 10

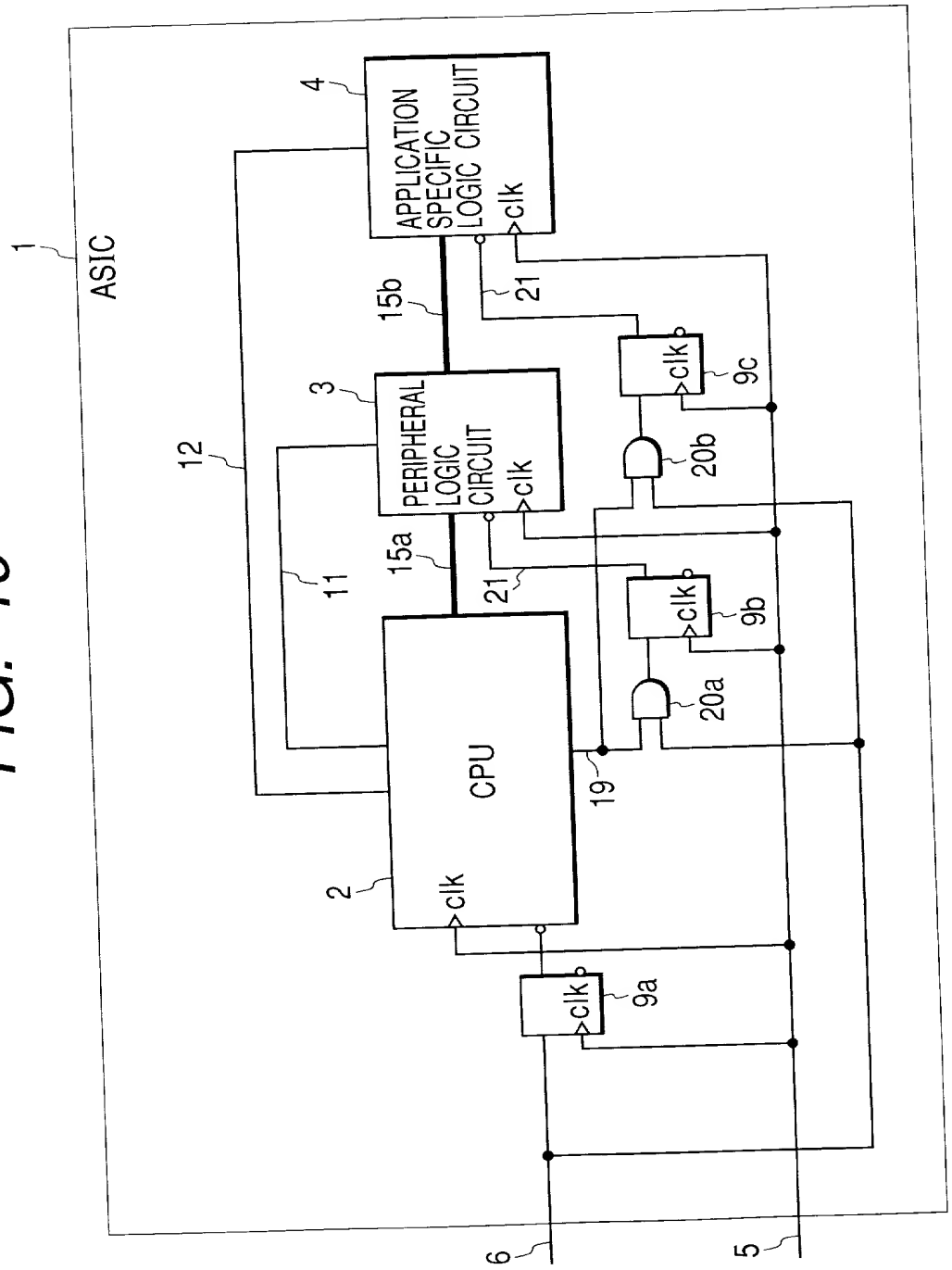
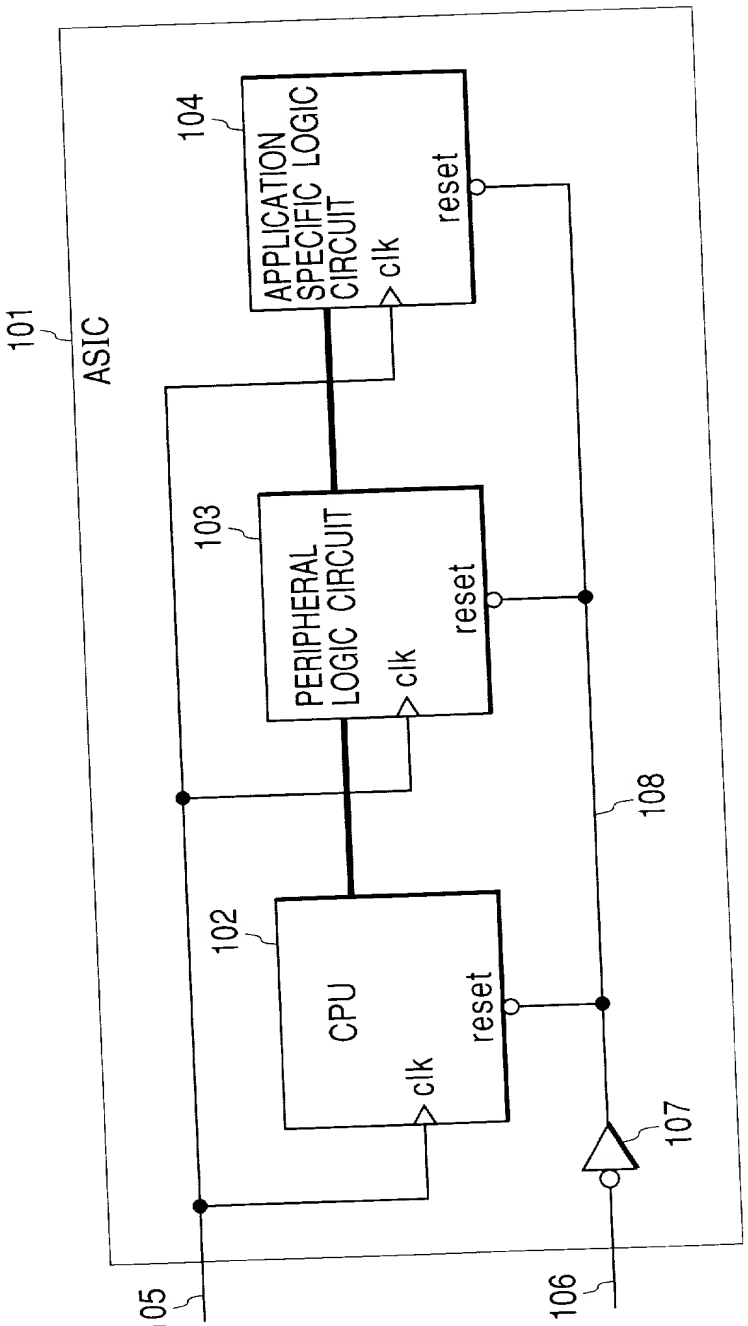

1
ASIC
4
APPLICATION SPECIFIC LOGIC CIRCUIT
clk
21
15b
3
PERIPHERAL LOGIC CIRCUIT
clk
12
11
15a
21
2
CPU
clk
19
clk
9c
20b
clk
9b
20a
clk
9a
6
5

FIG. 11


101
ASIC
104
APPLICATION SPECIFIC LOGIC CIRCUIT
clk
reset
103
PERIPHERAL LOGIC CIRCUIT
clk
reset
102
CPU
clk
reset
108
107
105
106